Professor Iain Thayne

The Ultrafast Systems Group at the University of Glasgow, Scotland have, for over a decade, been demonstrating advanced III-V High Electron Mobility Transistor (HEMT) and Monolithic MilliMetre-Wave Integrated Circuit (M³IC) technologies. This article summarises the latest developments in millimetre-wave HEMT technology reported by members of the Ultrafast Systems Group at the European Solid State Device Research Conference in Estoril, Portugal in September and at the October GAAS 2003 Conference in Munich .

Advanced III-V HEMTs

Millimetre-Wave Applications

The millimetre-wave bands cover the 30-300GHz range of the frequency spectrum. In this region exist a significant number of applications, including broadband radio communications; high data rate fibre systems; automotive collision warning; passive imaging; concealed weapon detection; passive imaging systems capable of 'seeing" through rain, snow and fog; environmental, atmospheric and pollution monitoring systems.

Many of these applications have operating frequencies of around 100GHz and above. A significant percentage of the markets are in the areas of imaging and sensing, where receiver sensitivity, determined primarily by the noise performance of the front-end low noise amplifier, where HEMTs outperform all other available technologies, is a key performance metric. Finally, there are numerous cases where imaging arrays would be the preferred system solution.

These requirements place huge demands on the active device and sub-system technologies for millimetre-wave applications in terms of inherent bandwidth and noise performance, but also require these parts be available in significant volumes at reasonable cost.

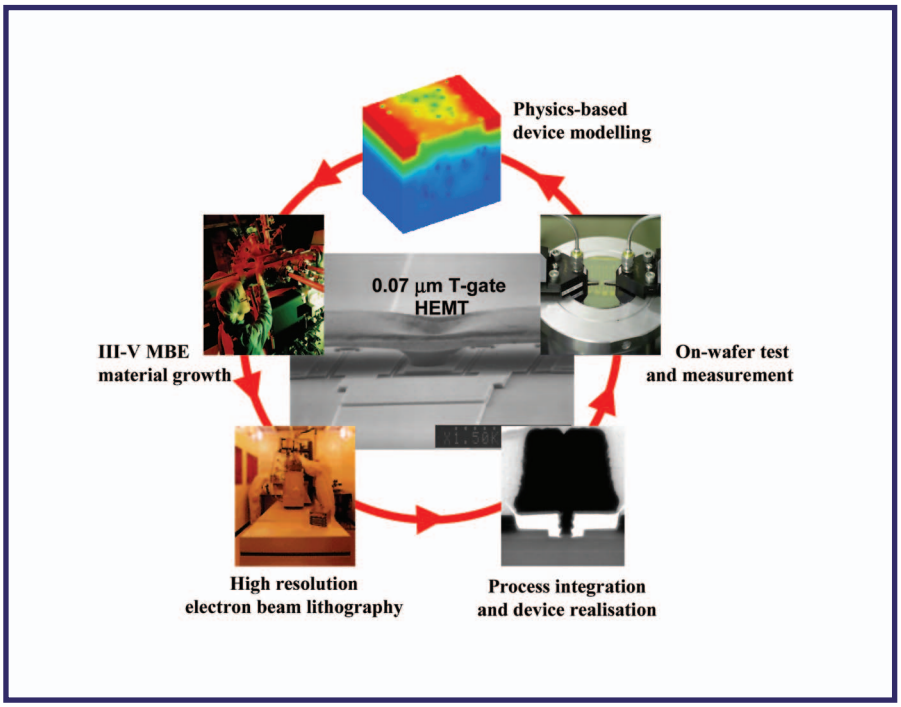

Figure 1 shows the 'virtuous circle' or close interplay between numerous research groups in the Nanoelectronics Research Centre at the University of Glasgow which all contribute to the realisation of advanced III-V HEMTs for millimetre-wave applications.

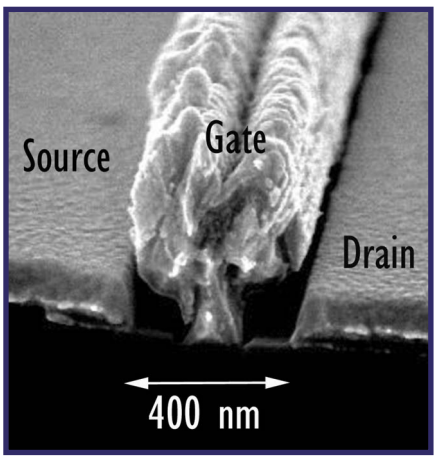

Figure 2 -120 nm footprint T-gate with self-aligned source and drain contacts.

The challenge for the device technologist therefore is to realise a manufacturable, high yield process where significant effort is taken to account for every last Ohm of resistance and FemtoFarad of capacitance, which at operating frequencies above 100 GHz have a huge impact on gain and noise performance (see Box 1 - What limits the performance of a millimetre-wave HEMT ?).

The Ultrafast Systems Group in Glasgow

The 12 strong Ultrafast Systems Group are involved in the design, fabrication and testing of a wide range of electronic components based on GaAs, InP and SiGe material systems for millimetre-wave applications requiring the very highest levels of performance.

The group is based in the University of Glasgow's Department of Electronics and Electrical Engineering and is part of the Nanoelectronics Research Centre.

What limits the performance of a millimetre-wave HEMT ?

Figure B1 shows a schematic cross section of a millimetre-wave HEMT device. Current flowing from source to drain in the device channel is modulated by varying the voltage applied to the Schottky gate contact. The key to the success of the HEMT is that the buried channel is formed in a high mobility layer which is spatially separated from the donor atoms which supply the channel charge. The device transconductance, gm, is a measure of the efficiency of channel current modulation as it is defined as the amount of channel current change for a given gate voltage modulation. To improve the channel current modulation efficiency, the gate is defined in a recess region with a tightly controlled geometry.

Having a large resistance located between the source and drain reduces the transconductance and therefore the channel current modulation efficiency. A 2-port lumped element equivalent circuit to predict the RF performance of a HEMT can be created based on the device geometry and vertical layer structure as shown in Figure B2.

From this, a number of RF figures of merit can be derived.

The device f^T is the frequency at which the short circuit current gain falls to unity. This can be related to the lumped element parameters via the expression

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

where (Cgs + Cgd) is the total capacitance associated with the Schottky gate contact.

From this, it can been seen that to achieve a high f_T, the device must have a large transconductance and small gate capacitance, the latter being achieved by the definition of a short gate length which for millimetre-wave applications should be less that 0.15µm.

A second RF figure of merit, *fmax*, is related to the frequency at which the device power gain falls to unity. This can be related to the equivalent circuit elements via the expression

$$f_{max} = \frac{f_T}{2\left(\frac{R_g + R_i + R_s}{R_{ds}} + \left(2\pi f_T R_g C_{gd}\right)\right)^{\frac{1}{2}}}$$

This shows that to achieve useful power gain at high frequencies, the device must first have a large fT, but in addition have small source, drain and gate resistances. This means reducing the resistance associated with accessing the intrinsic device under the gate, and forming a small geometry gate with a low resistance, achieved using the T-gate structure shown schematically above, and in practice in Figure 2 in the main text.

A third figure of merit is the noise figure NF_o, which at a given frequency *f*, can be defined as

$$NF_o = 2\pi f C_{gs}\sqrt{\frac{(R_g + R_s)}{g_m}}$$

This again demonstrates the importance of having a large transconductance, short gate low capacitance device with minimal source, drain and gate resistances.

For further information: the interested reader is referred to "*RFIC and MMIC design and technology.*" Edited by I.D. Robertson, S. Lucyszyn, IEE Press, ISBN 0 85296 786 1, 2001

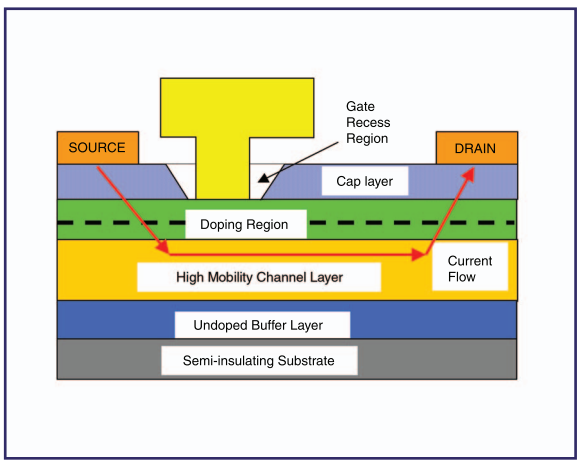

Figure B1 – Cross section of a millimetre-wave III-V HEMT device. Current flows from the source to the drain in the high mobility buried channel under the Schottky gate contact. The gate sits in a recess to improve the current modulation in the device.

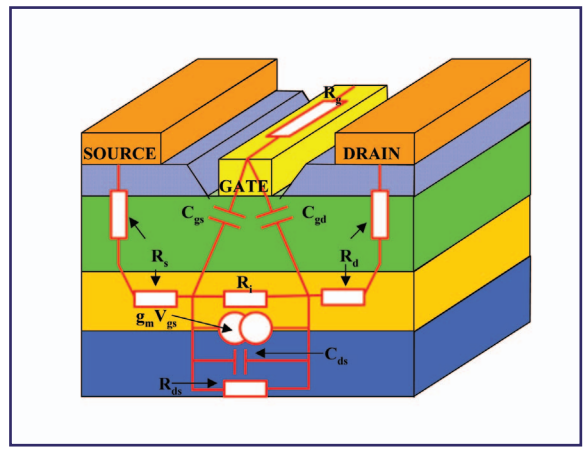

Figure B2 – Lumped element equivalent circuit mapped onto the physical structure of a millimetrewave III-V HEMT. From this equivalent circuit, a number of RF figures of merit can be derived. The challenge in optimising a III-V HEMT for millimetre-wave applications is to minimise various elements in the equivalent circuit such as the source and drain resistances, Rs and Rd and the gate resistance Rg.

Figure 3 - Comparative DC and RF performance metrics of conventional and self-aligned sub-100nm InP HEMTs

Device Type	Drive Current (mA/mm)	gm (mS/mm)	fT (GHz)	fmax (GHz)
Conventional	850	1300	255	420
Self-aligned	900	1550	270	430

Other groups in the Department include a large physics-based device modelling activity, a team of experts in III-V molecular beam epitaxy (MBE) and a very large multi-disciplinary group of technologists working in the area of high resolution nanofabrication, including direct-write electron beam lithography and high aspect ratio dry-etching.

As a result, the Ultrafast Systems Group has access to a complete in-house capability for the realisation of advanced sub-100 nm III-V HEMTs, leading to the Glasgow "virtuous cycle" of device development illustrated in Figure 1, where device optimisation can continually be achieved by feedback to and interaction with, modellers, growers and technologists.

Recent Advances

The devices described in the recent Ultrafast Systems Group ESSDERC and GAAS 2003 papers focus on two distinct areas of III-V HEMT process development described in more detail below.

1) Low thermal budget, self-aligned gate processes

As shown in Box 1, parasitic access resistance at the source and drain sides of the HEMT degrade both gain and noise performance. This can be minimised by reducing the source-drain separation, or in the most extreme situation, by self-aligning the source and drain "Ohmic" contacts to the gate as shown in Figure 2.

Adopting such a solution has a number of effects however. First, the source and drain Ohmic contact metallisation has to be thinner than the "stalk" of the HEMT T-gate to avoid short-circuiting the device. Second, the thermal budget for the formation of low resistance Ohmic contacts (a process typically carried out at around 300°C) is incompatible with a pre-existing gate metallisation in many processes, as gate "sinking" leading to reduced device lifetime and reliability will result.

The solution therefore, requires the development of a thin, low thermal budget source and drain contact strategy, whilst maintaining a low access resistance to the device to exploit the performance advantages offered by moving to a self-aligned gate approach.

In the Ultrafast Systems Group work presented at ESSDERC and GAAS 2003, 120nm and 70nm gate length InP-based HEMTs realised using a low contact resistance self-aligned gate approach, based on a completely non-alloyed Ohmic contact strategy, were described.

The realisation of devices of this type were made possible by optimisation of both the Ohmic contact composition and thickness, but equally importantly by careful design and MBE growth of a novel vertical layer architecture, specifically chosen to minimise the resistance into the device channel from the cap layer (See Box 1 for further background). This work benefited enormously from the close interaction between MBE material growers, device technologists and device modellers and is an excellent example of the Glasgow "virtuous cycle" in operation.

A comparison of key DC and RF figures of merit was presented for self-aligned and "conventional" devices realised in the same batch (see Box 1 for more details on HEMT figures of merit). These are summarised in Figure 3, from which a number of points are clear.

The self-aligned devices outperform the "conventional" devices in terms of transconductance, f_T and f_{max}, showing that the strategy does indeed deliver improved performance, and is not negatively impacted by the non-annealed Ohmic contact strategy. In addition, both device types demonstrate large drive currents reflecting the doping strategies adopted in the vertical architecture to minimise cap to channel resistance. The RF performance metrics indicate their applicability in applications beyond 100GHz.

2) High uniformity "digital etching" at the 50nm node

One of the key aspects of a III-V HEMT is the geometry of the recess trench in which the gate sits (See Box 1). The depth of the etch trench determines the device threshold voltage, with tight control only achievable using etching techniques that are precise to a few nanometres. Such etching techniques do exist, and take advantage of selectively removing one layer of a vertical architecture, stopping on a second layer. The most successful of these types of etch are wet chemical, which often require careful control of temperature,

Figure 5 – Comparison of 50nm pseudomorphic GaAs HEMTs containing device channel with 22% indium content and 50nm metamorphic GaAs HEMTs with 53% indium concentration in the device channel. Both devices are suitable for applications at 100 GHz and beyond, and have been realised with yields in excess of 96% with high uniformity.

Device Type	Device channel indium concentration	gm (mS/mm)	fT (GHz)	fmax (GHz)
Pseudomorphic GaAs HEMT	22%	610	200	280
Metamorphic GaAs HEMT	53%	1550	350	400

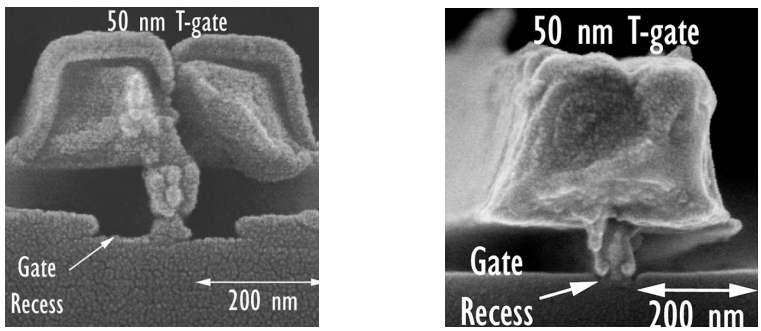

Figure 4 – showing the lateral etching control offered by "digital" recess etching. In both micrographs, the depth of the recess is 30 nm. The micrograph on the left shows a "wide" gate recess with large lateral extent whilst the micrograph on the right shows a recess tightly defined around the gate footprint.

pH and composition however, and give reduced flexibility in vertical architecture design and optimisation.

In addition, the lateral etching of the recess trench impacts the device access resistance, and so the drive current transconductance and thereby the millimetre-wave gain and noise performance. Further, the recess trench geometry and lateral extent plays a major role in determining the breakdown characteristics of a III-V HEMT, particularly in sub-100 nm gate length devices.

At both ESSDERC and GAAS 2003, the Ultrafast Systems Group presented results on a range of GaAs-based HEMTs with gate lengths of 50nm. The gate recess was formed using a novel "digital" wet chemical etch. As will be shown below, the devices demonstrated impressive DC and RF performance metrics, but equally importantly in terms of meeting end-user requirements, very high yield and uniformity.

"Digital" etching is a simple wet etching technique that involves oxidising the surface of a IIIV semiconductor in a controlled manner followed by removal of the surface oxide in the etching step. Digital etching is capable of giving nanometre level etch depth precision, with lateral etching control easily incorporable. As it is not a selective etch chemistry, digital etching works across material systems and is more transferable into a manufacturing environment, as it does not require the same levels of pH or temperature control.

Figure 4 shows the typical range of lateral control achievable with digital etching for HEMT T-gates with critical features down to 50nm.

Figure 5 summarises the DC and RF results presented at ESSDERC and GAAS 2003 for IIIV HEMTs by the Ultrafast Systems Group.

As expected, the higher indium concentration in the channel of the GaAs metamorphic HEMTs results in improved performance, comparable with similar geometry InP-based HEMTs. Both sets of devices demonstrate performance suitable for the realisation of 100GHz M^3ICs.

In addition, the wafer runs leading to these 50nm gate length devices resulted in 96% functional yield with threshold voltage variations of around 35 mV, indicating both the high yield and uniformity of the digital etching processes.

Conclusion

In their recent presentations the Ultrafast Systems Group at the University of Glasgow have demonstrated a range of advanced III-V HEMT technologies with feature sizes down to 50nm with high performance metrics, uniformity and yield as required for a wide range of millimetre-wave applications including array based imaging and sensing beyond 100 GHz.

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Further Details

For further details on the work of the Ultrafast Systems Group, contact Professor Iain Thayne on +44 141 330 3859. Email: ithayne@elec.gla.ac.uk or at www.ufast.org

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